

Body Biasing Injection: Triple or Dual Well?

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CONTEXT & STATE OF THE ART

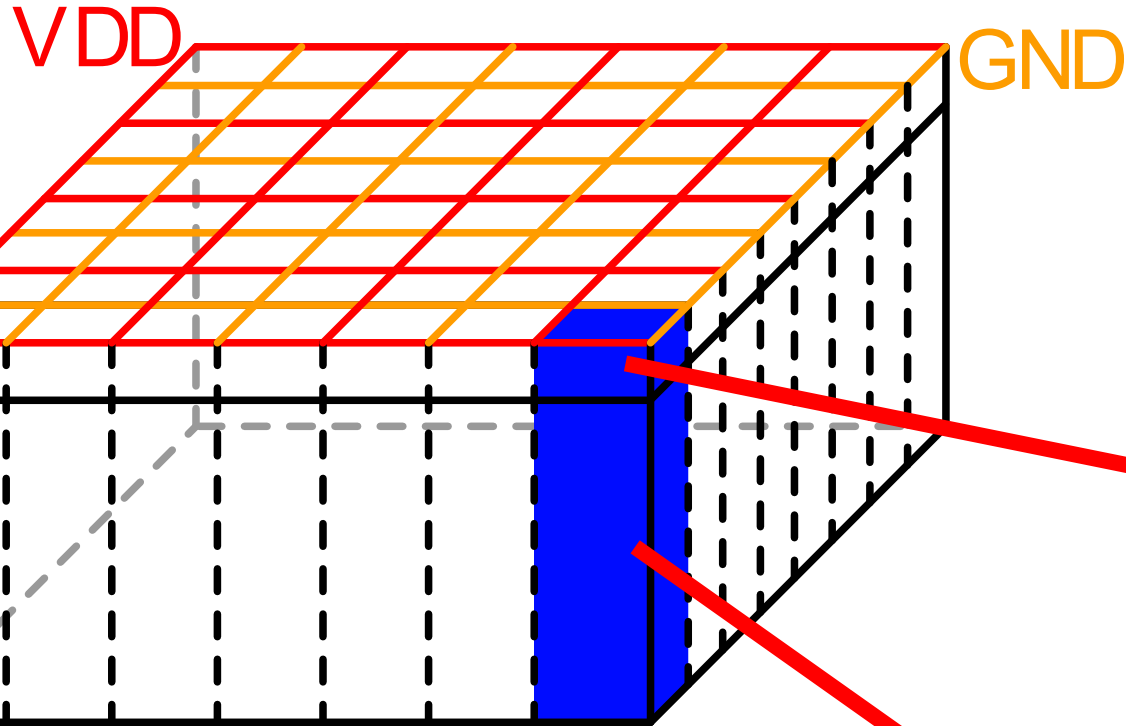
- Fault injection techniques: VGFI, EMFI, LFI, BBI
- State of the art:
 - *Philippe Maurine et al. (2012), "Yet Another Fault Injection Technique : by Forward Body Biasing Injection" YACC'2012, lirmm-00762035*
 - *K. Tobich et al. (2013), "Voltage Spikes on the Substrate to Obtain Timing Faults", doi: 10.1109/DSD.2013.146*
 - *Noemie Beringuier-Boher et al. (2016), "Body Biasing Injection Attacks in Practice", doi: 10.1145/2858930.2858940*
 - *O'Flynn Colin. (2021) "Low-Cost Body Biasing Injection (BBI) Attacks on WLCSP Devices", doi: 10.1007/978-3-030-68487-7_11*
 - *G.Chancel et al. (2022), "Body Biasing Injection: To Thin or Not to Thin the Substrate? doi: 10.1007/978-3-030-99766-3_6*
 - *T. Wadatsumi et al. (2022), "Voltage Surges by Backside ESD Impacts on IC Chip in Flip Chip Packaging" doi: 10.1109/IRPS48227.2022.9764457*

OBJECTIVES

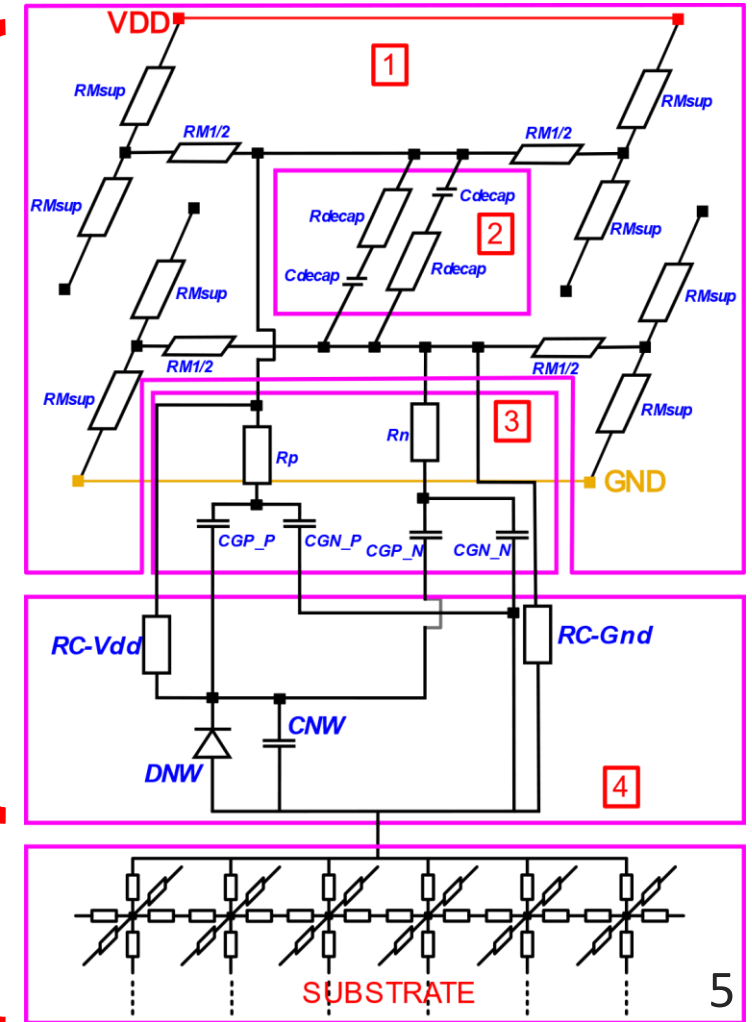
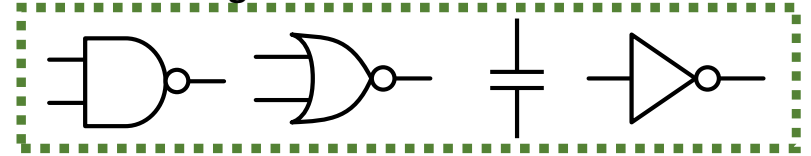
- Improve electrical model while evaluating **Dual-Well** and **Triple-Well** ICs
 - Efficiency differences?
 - Body diode biasing differences
- To address this:
 - **Dual-Well** and **Triple-Well** models
 - Experimental observation

SIMULATION ANALYSIS

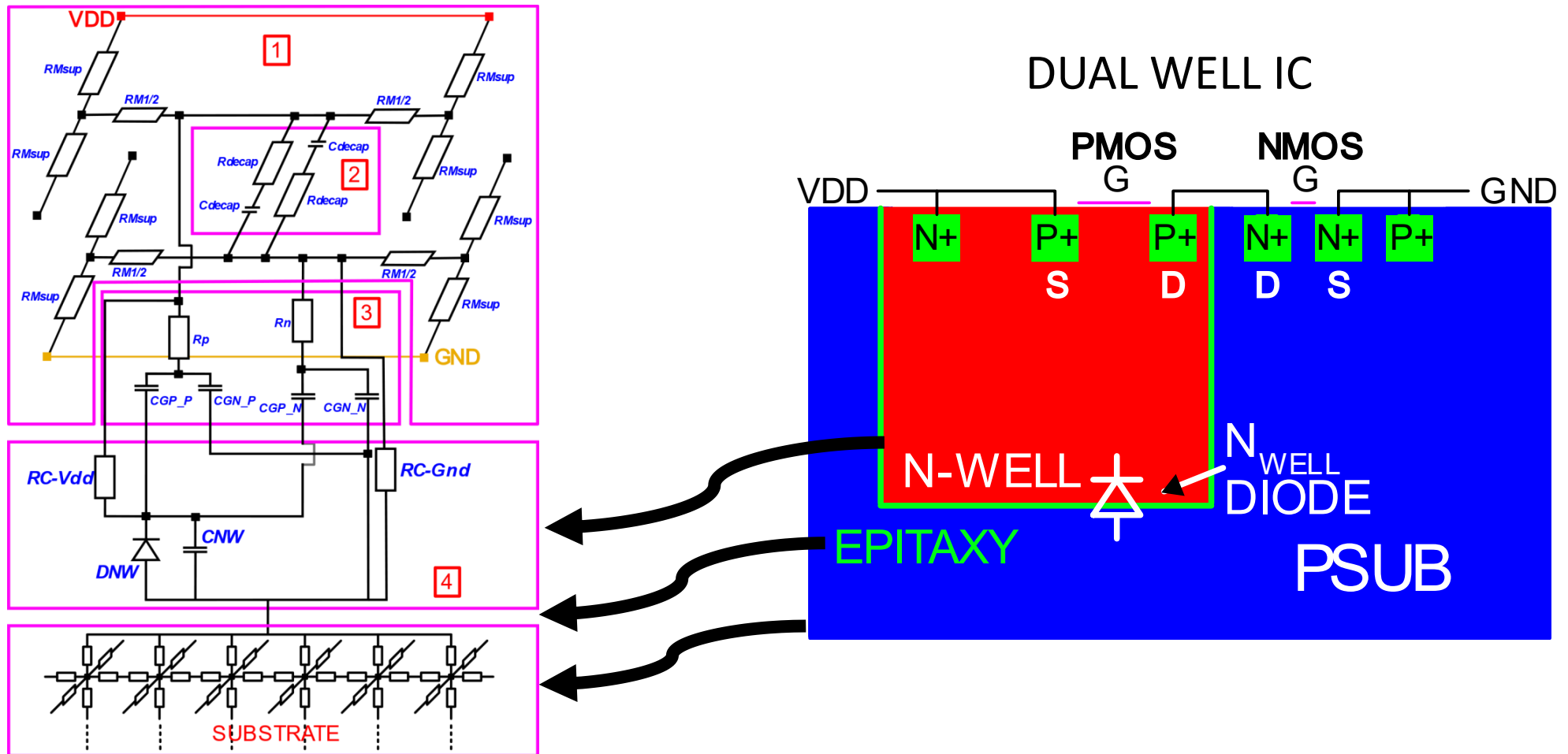
SIMULATION ANALYSIS



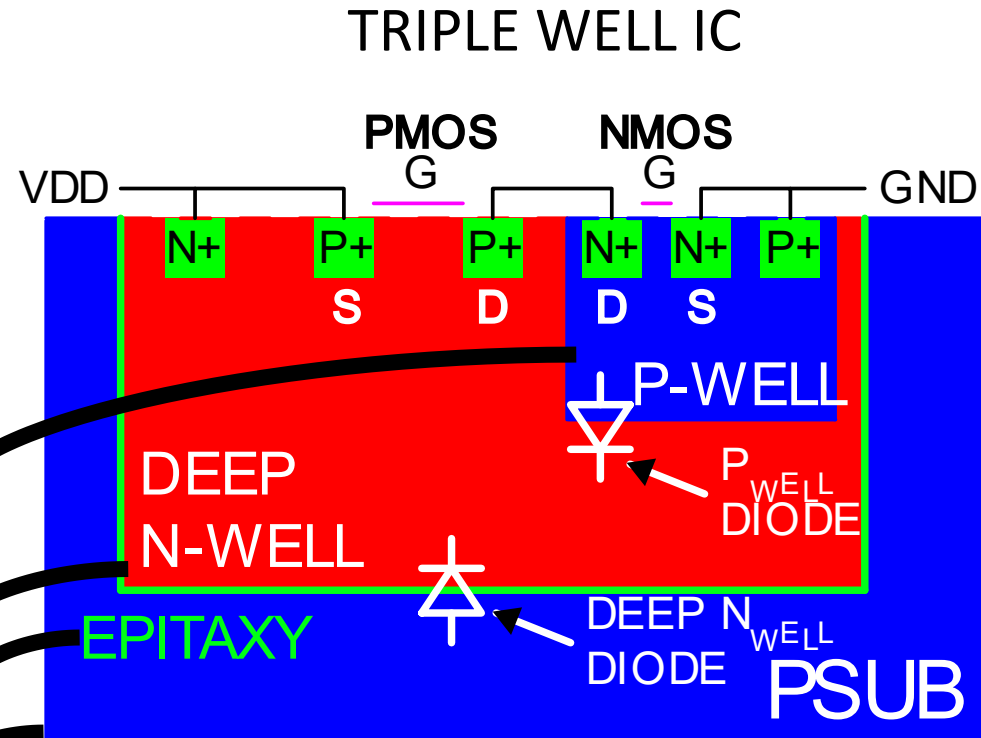
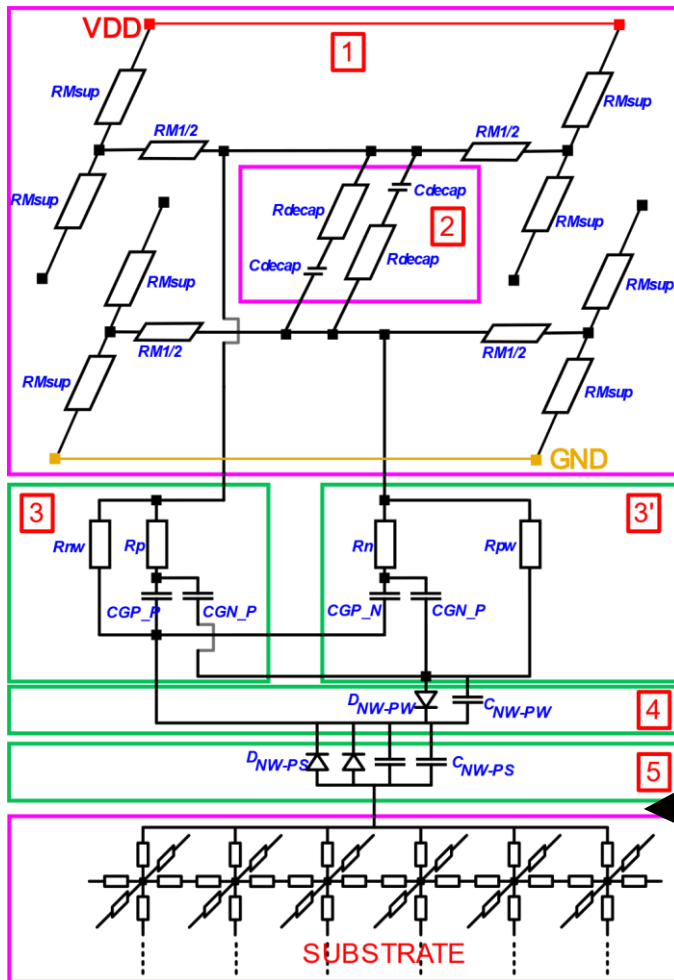
A segment of a standard cell row



SIMULATION ANALYSIS: DUAL WELL IC

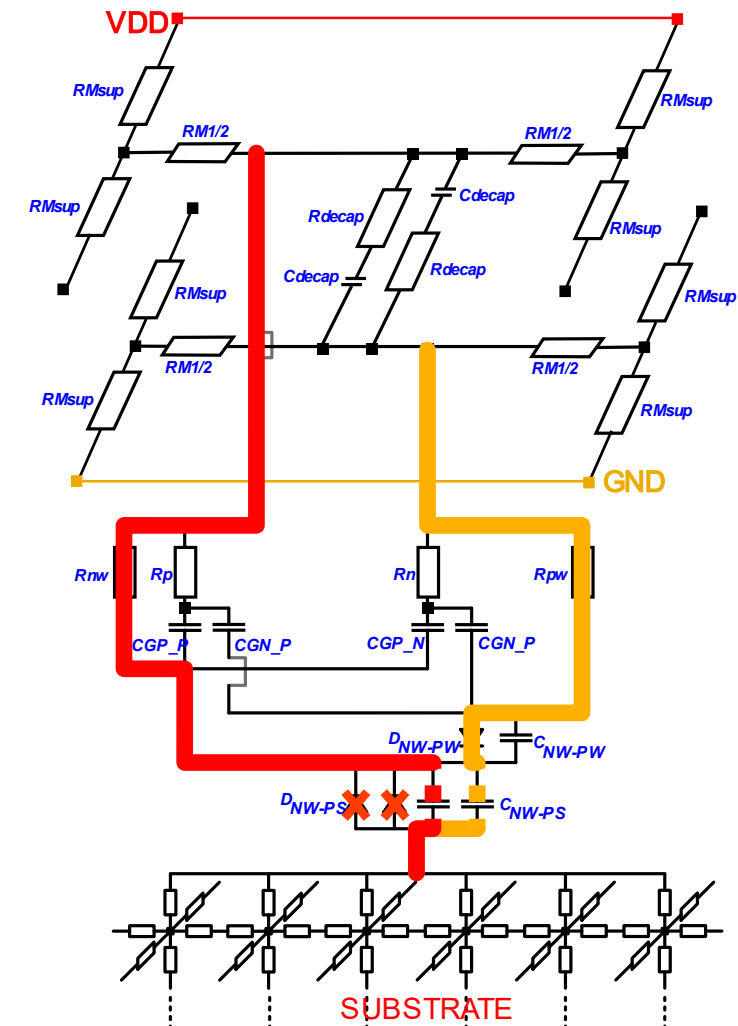
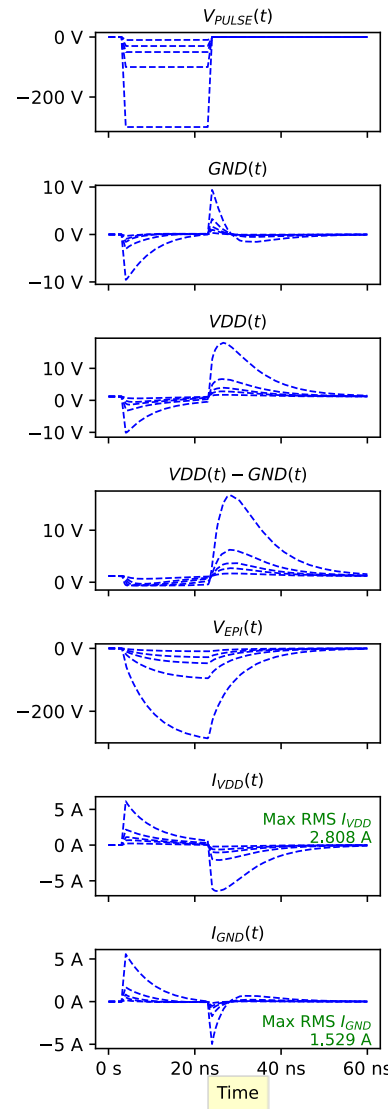
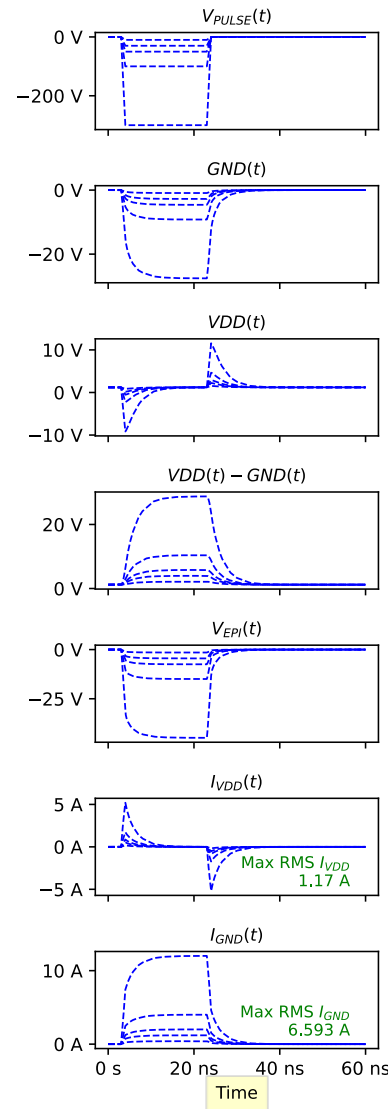
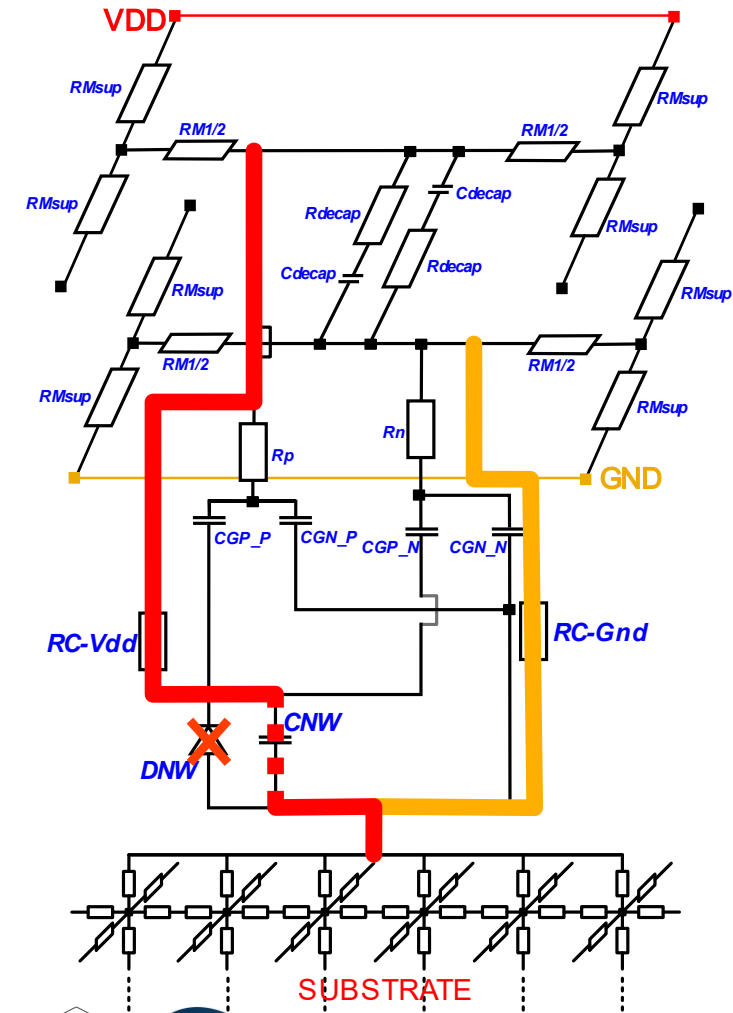


SIMULATION ANALYSIS : TRIPLE WELL IC

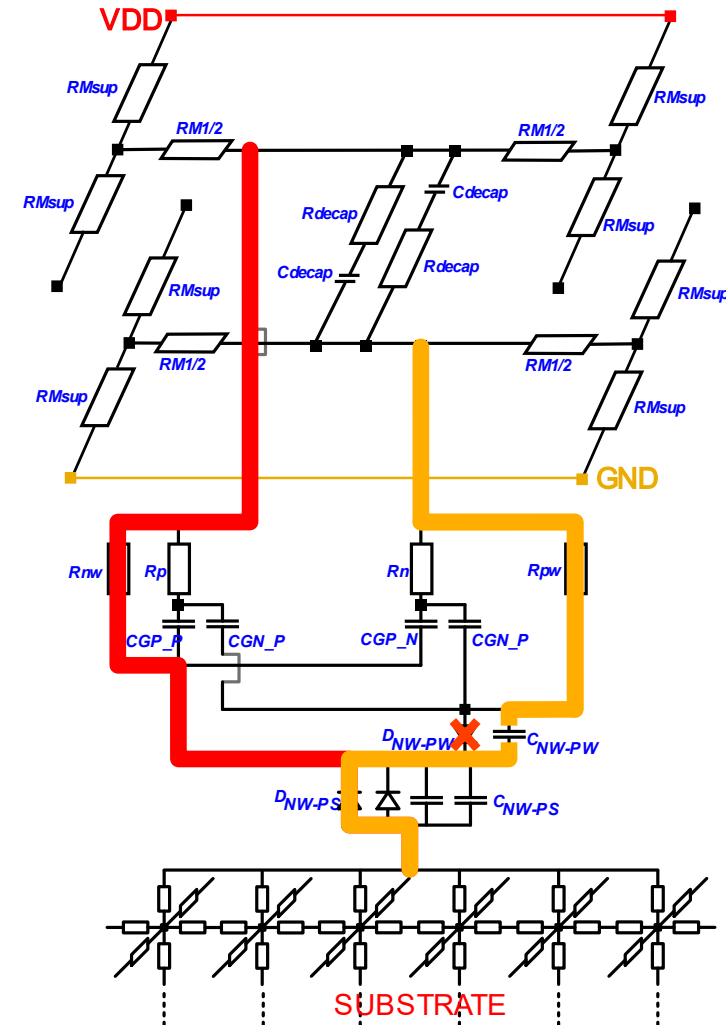
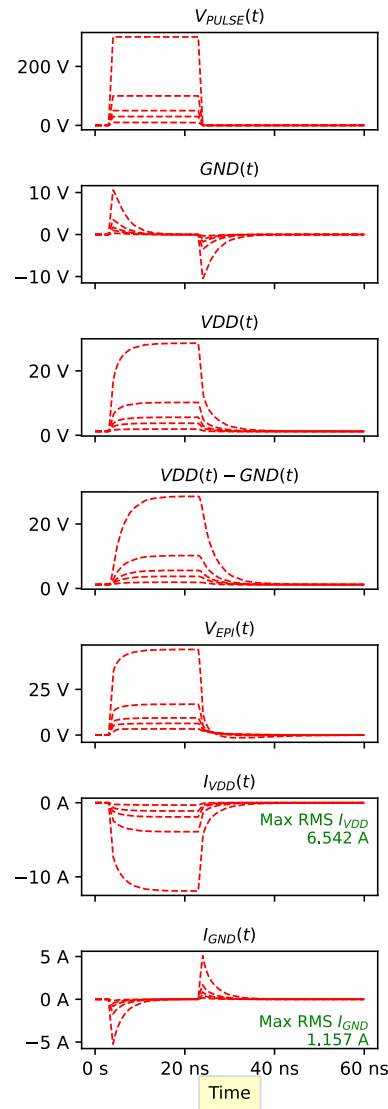
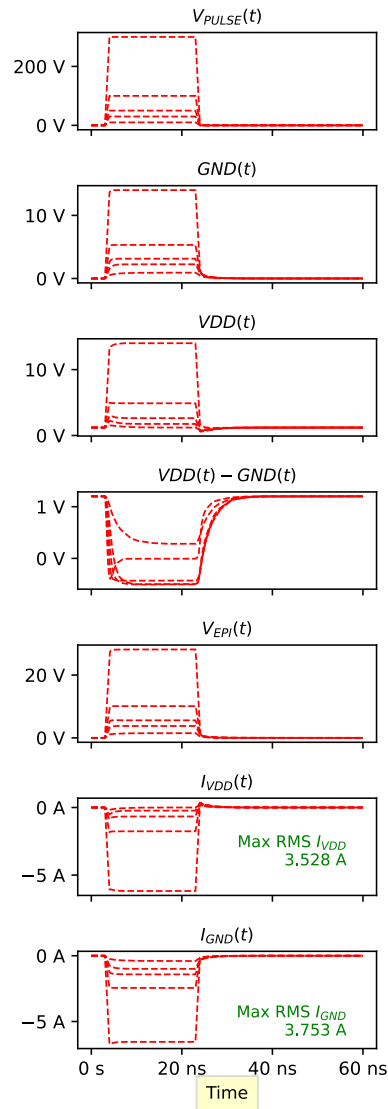
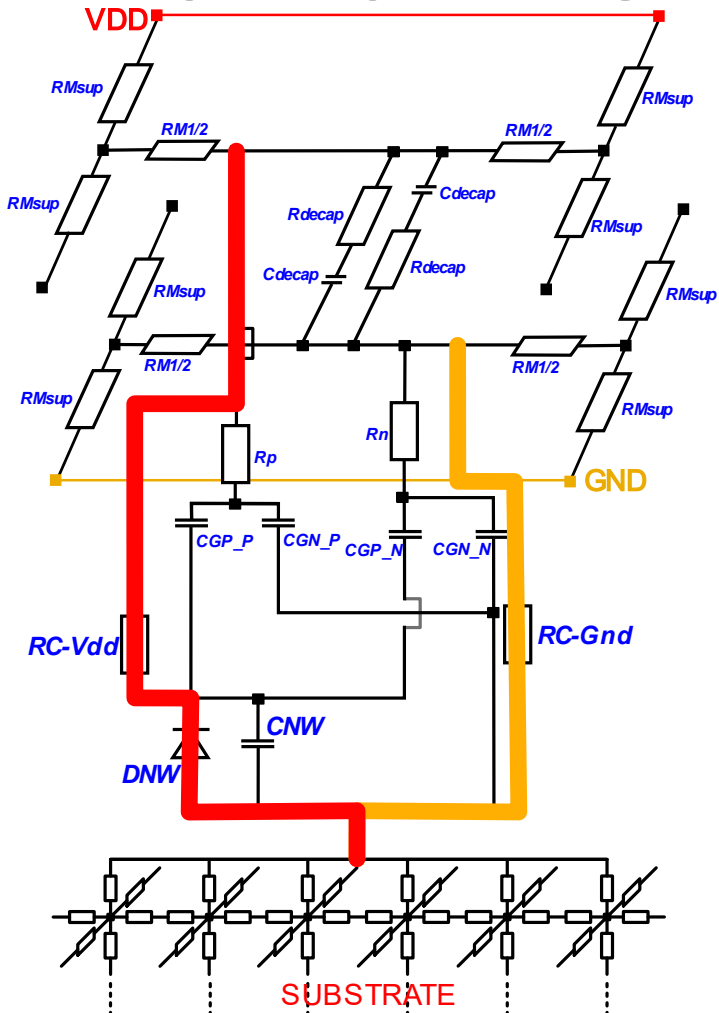


SIMULATION ANALYSIS: POWER RAILS

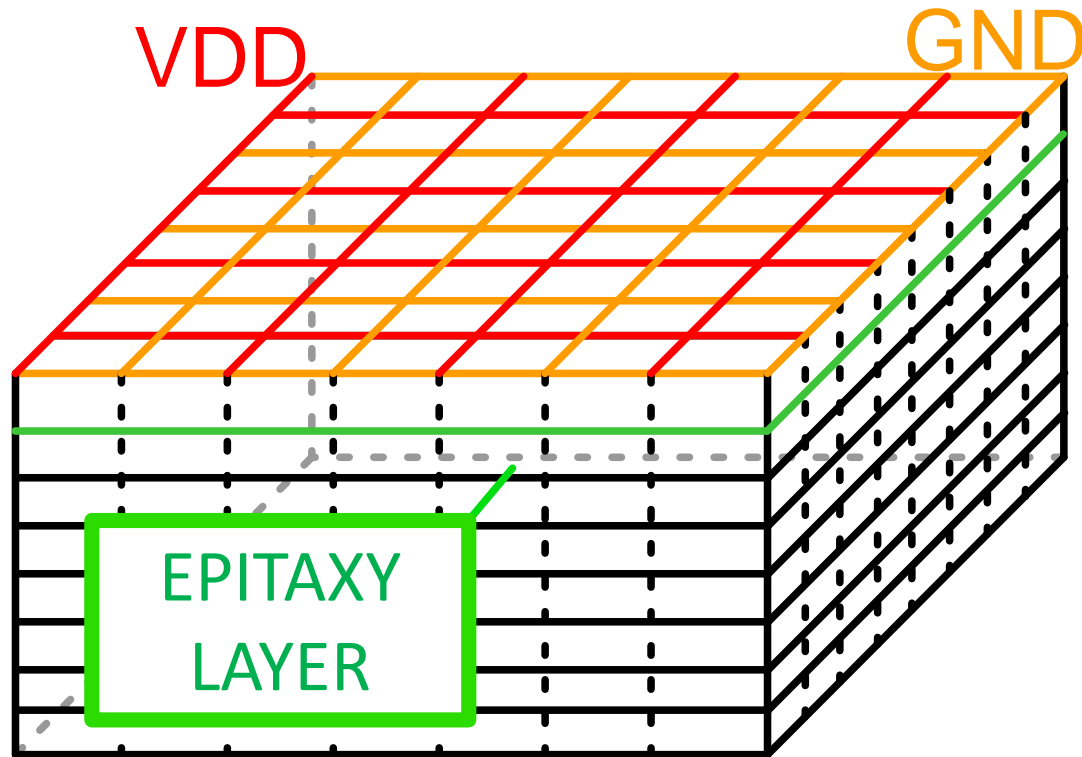
SIMULATION ANALYSIS: NEGATIVE PULSES



SIMULATION ANALYSIS: NEGATIVE PULSES

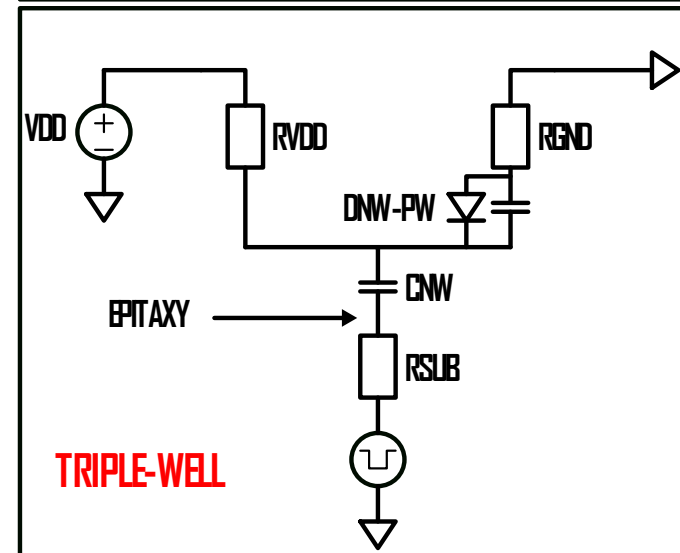
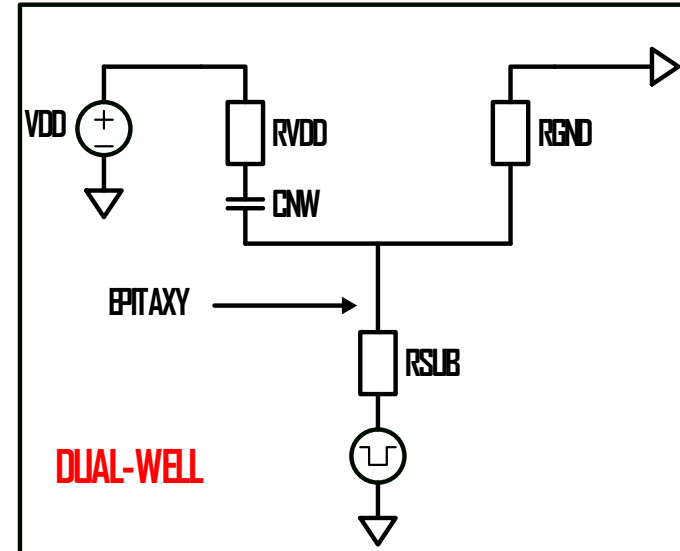
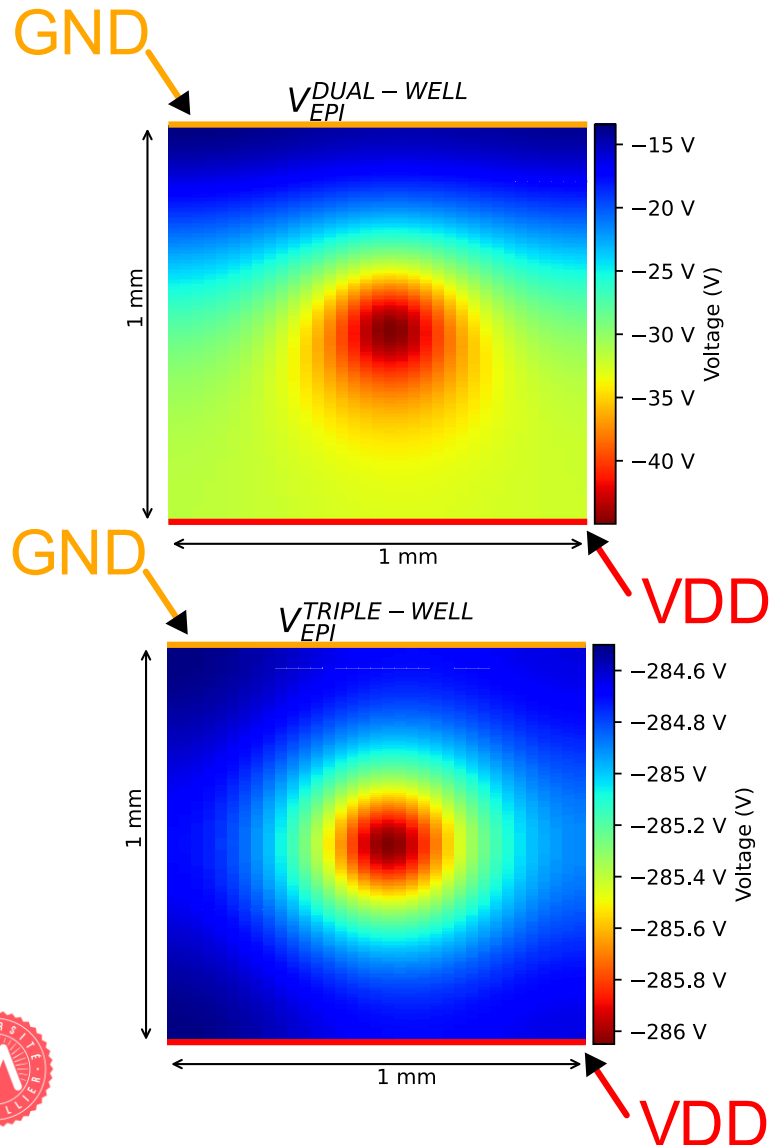


SIMULATION ANALYSIS: SUBSTRATE ANALYSIS



- EPITAXY VOLTAGE REPARTITION
- NEGATIVE PULSE
- 300 V
- 20 ns
- SECOND EDGE OF THE PULSE

SIMULATION ANALYSIS: SUBSTRATE ANALYSIS

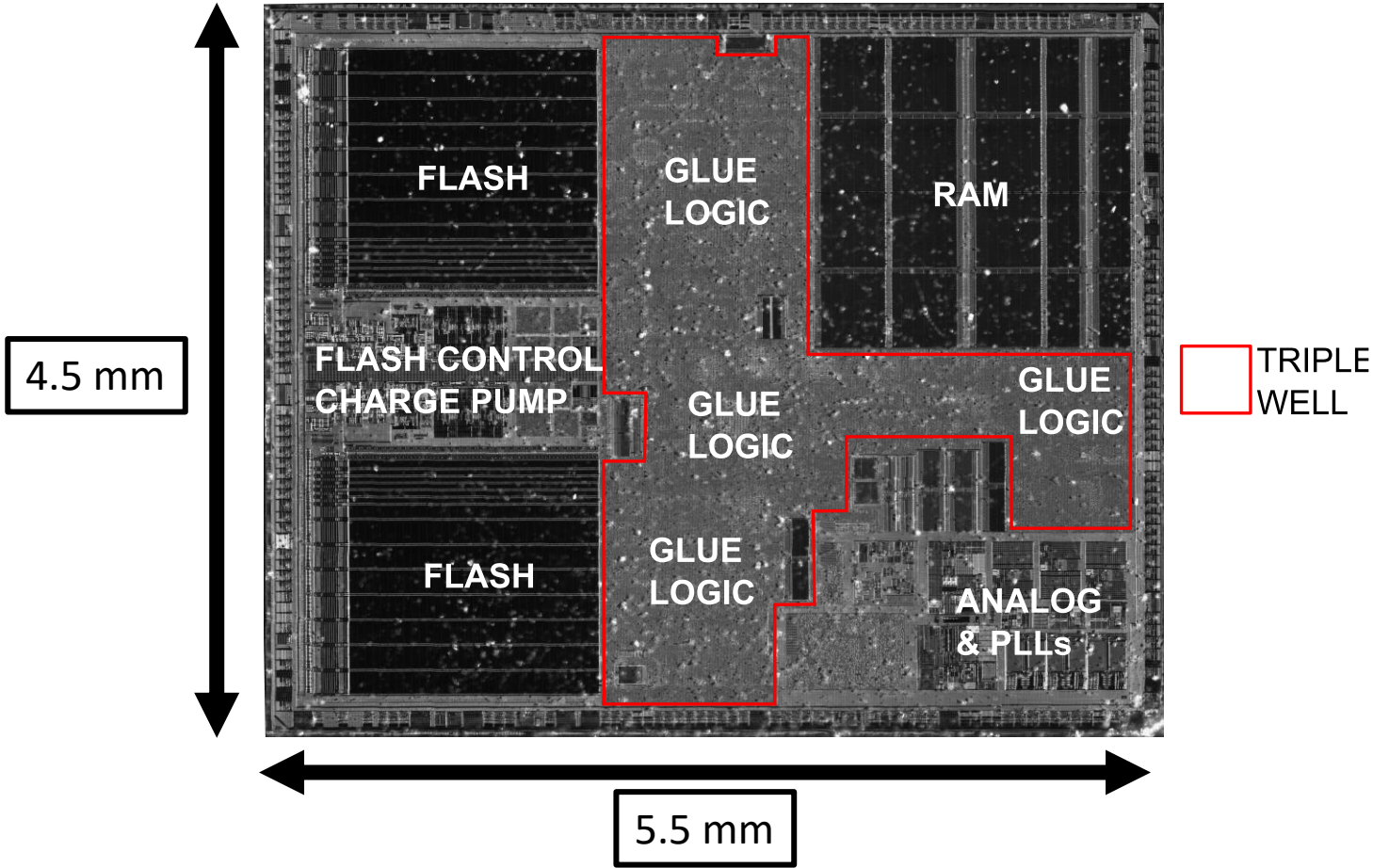


EXPERIMENTAL OBSERVATION

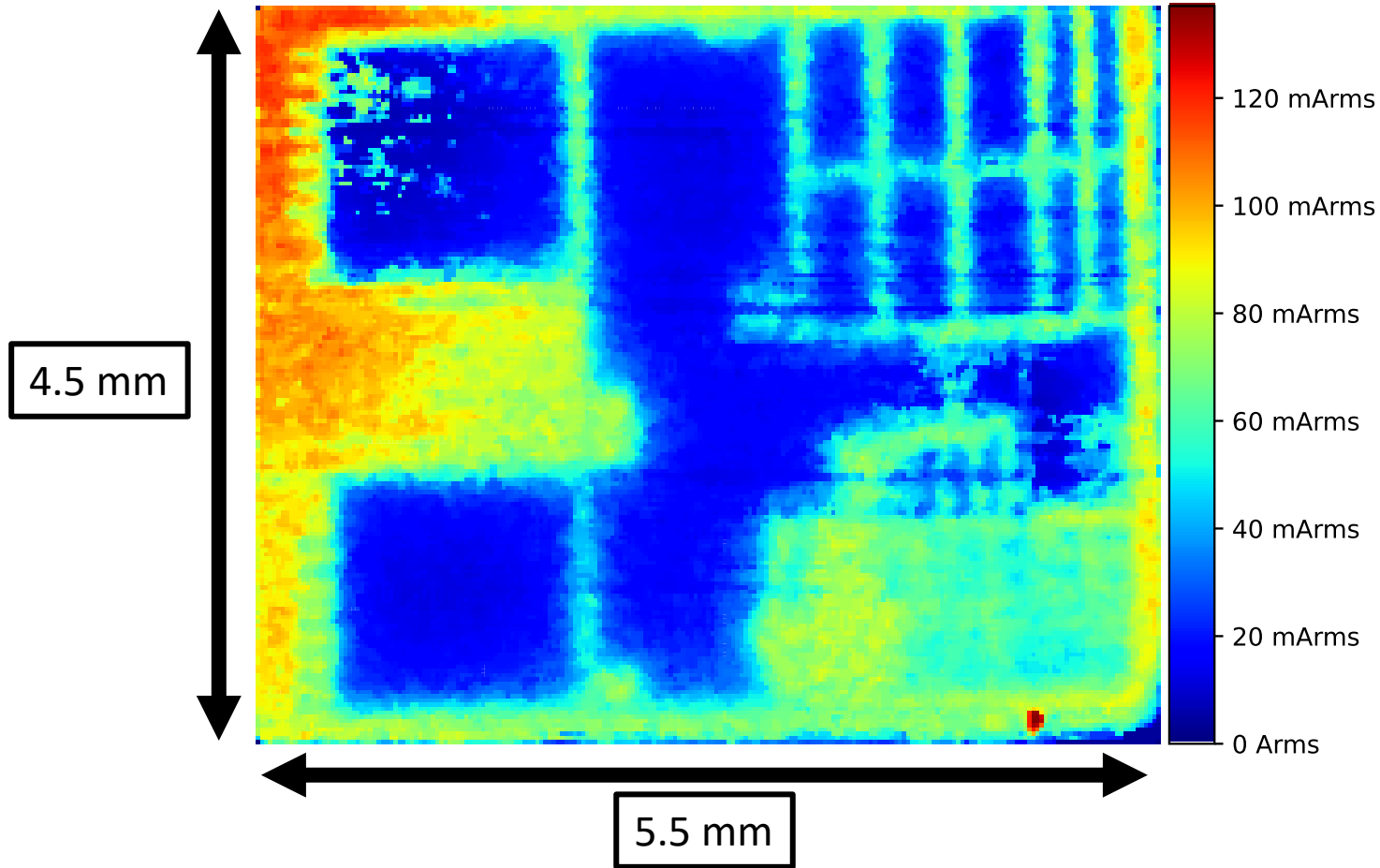
EXPERIMENTAL OBSERVATION

- Test platform:
 - Voltage pulse generator:
 - Amplitude: $\pm 50\text{V}$ to $\pm 750\text{V}$
 - Pulse Width: 6 ns to 20 ns
 - Custom BBI probes:
 - 3D printed part
 - Spring-loaded pin
 - Modern 90 nm microcontroller

EXPERIMENTAL OBSERVATION

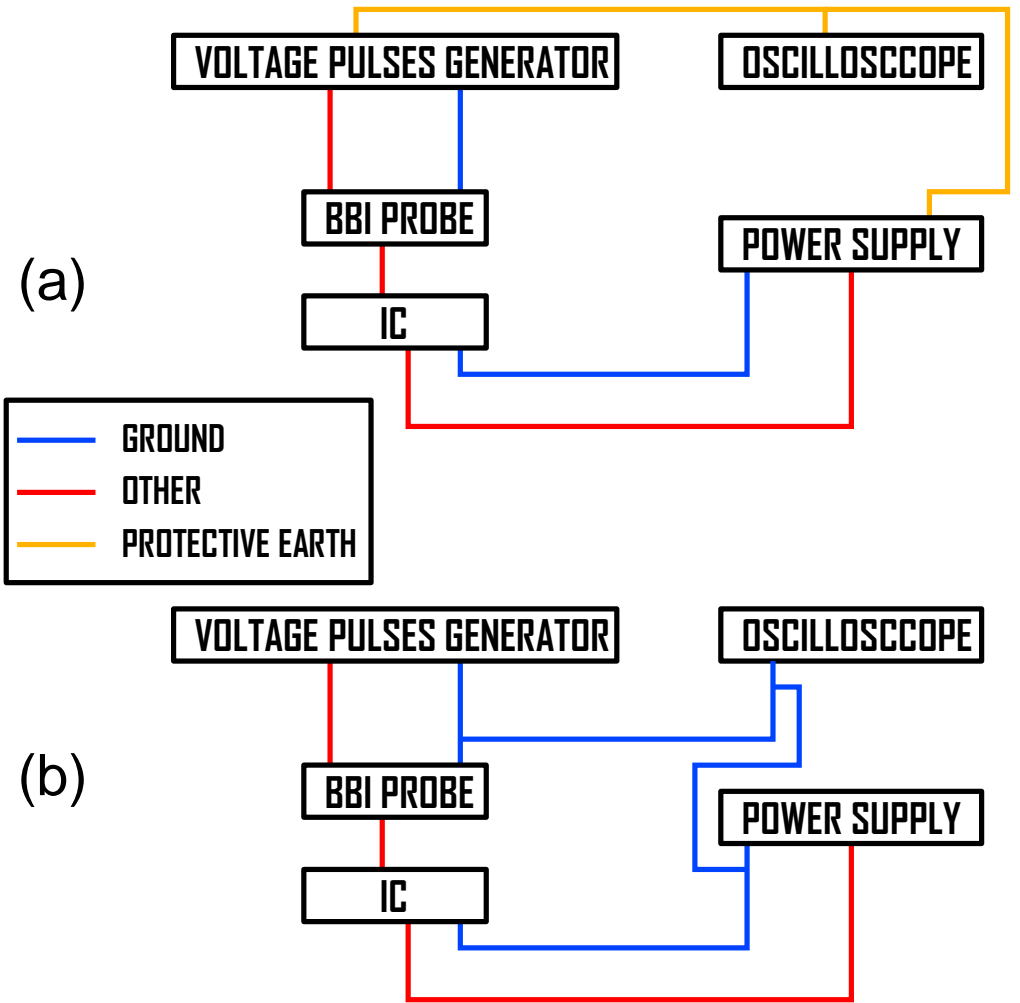
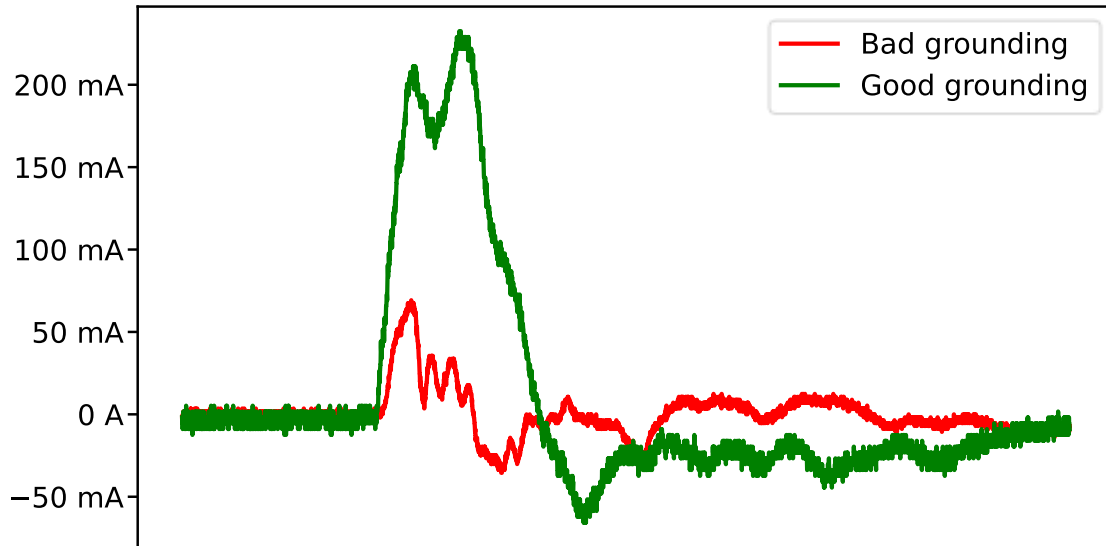


EXPERIMENTAL OBSERVATION

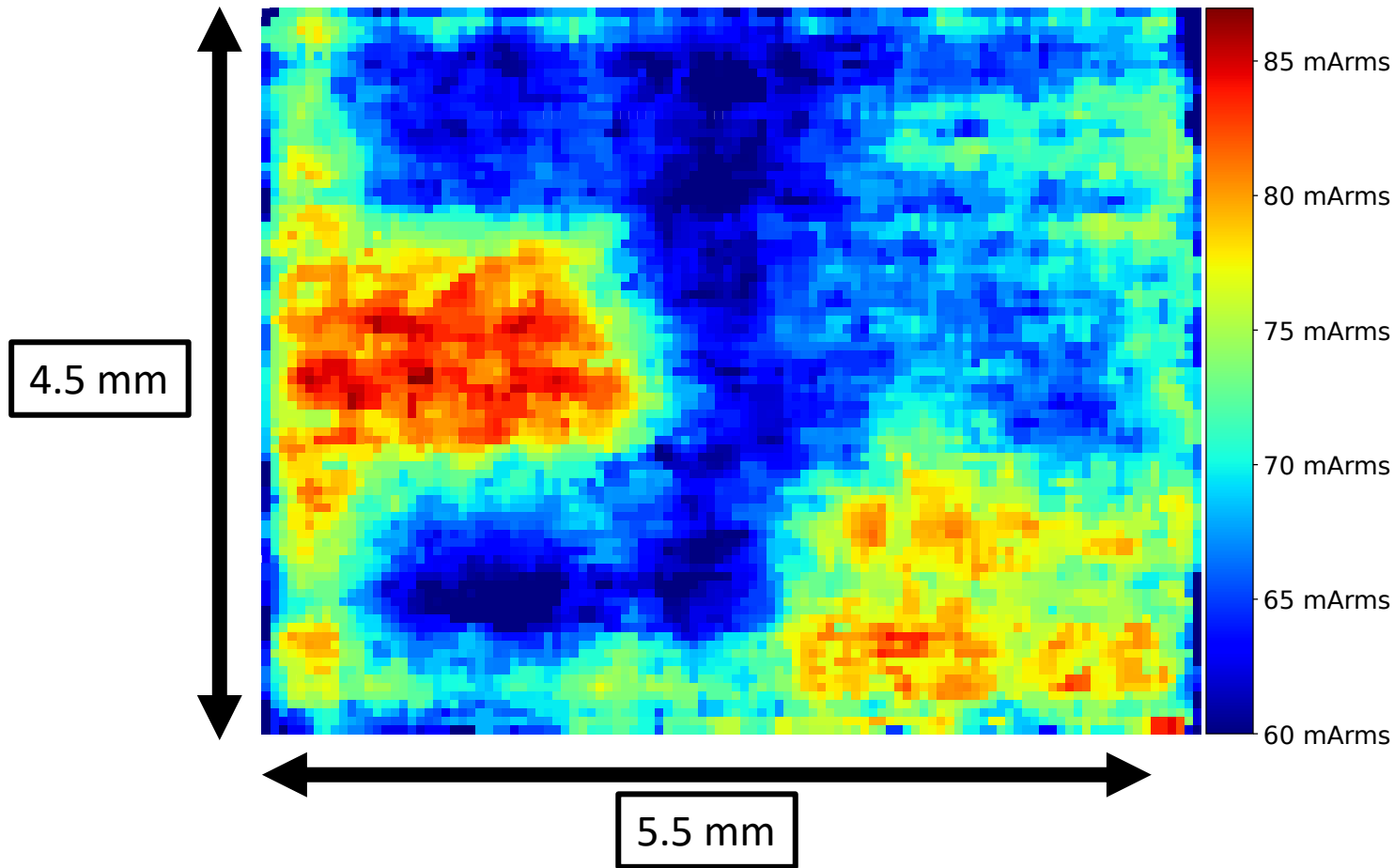


- FLOORPLAN CARTOGRAPHY
- 50 μm SUBSTRATE THICKNESS
- NEGATIVE PULSE
- Amplitude: 70 V
- Pulse width: 20 ns
- CURRENT THROUGH μCU **GND**

EXPERIMENTAL OBSERVATION



EXPERIMENTAL OBSERVATION



- **IMPROPER GROUNDING**
- FLOORPLAN CARTOGRAPHY
- 50 μm SUBSTRATE THICKNESS
- NEGATIVE PULSE
- Amplitude: 70 V
- Pulse width: 20 ns
- CURRENT THROUGH μCU **GND**

CONCLUSION

- Differences between types of substrate?
- Different effects on the power rails
- Polarity is critical
- Dual-well and triple-well react differently
- Equipment grounding is critical